AAT2522

SwitchReg™

Dual High-Current, Low-Noise, Step-Down Regulators

General Description

The AAT2522 SwitchReg is a dual high-current step-down converter with an input voltage range of 2.7V to 5.5V and an adjustable output voltage from 0.6V to V_{IN}. The 1.4MHz switching frequency enables the use of small external components. The compact footprint and high efficiency make the AAT2522 an ideal choice for portable applications.

The AAT2522 delivers load currents up to 3.0A maximum output current per regulator. Ultra-low $R_{DS(ON)}$ integrated MOSFETs and 100% duty cycle operation make the AAT2522 an ideal choice for high output-voltage, high current applications which require a low dropout threshold.

The AAT2522 provides excellent transient response and high output accuracy across the operating range. The AAT2522's unique architecture requires no external compensation components, and produces reduced ripple and spectral noise. Over-temperature and short-circuit protection safeguard the AAT2522 and system components from damage.

The AAT2522 is available in a Pb-free, space-saving 16-pin 3mm x 4mm TDFN package. The product is rated over an operating temperature range of -40°C to +85°C.

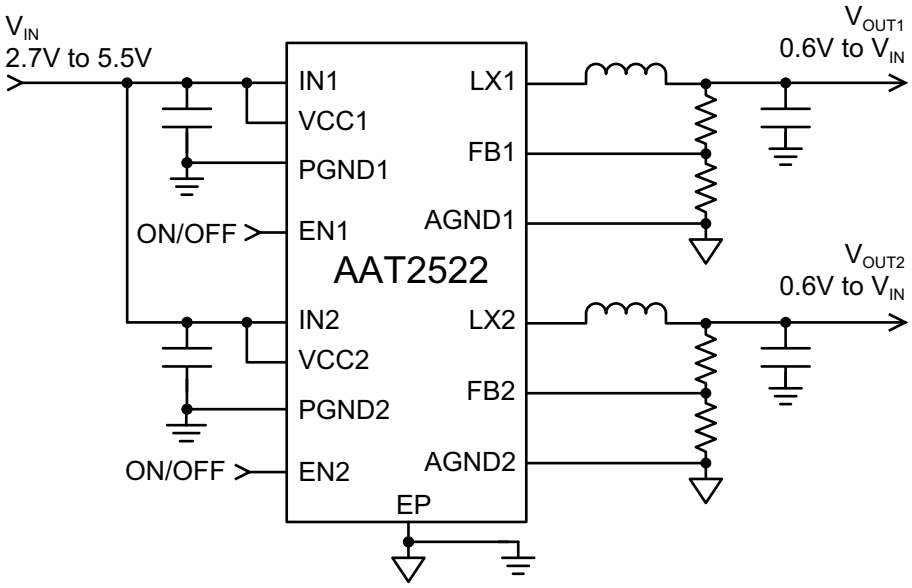
Features

- Dual 3.0A Peak Output Current Regulators
- 2.7V to 5.5V Input Voltage Range
- Adjustable Output Voltage (0.6V to V_{IN})
- 100% Duty-Cycle, Low-Dropout Operation
- Integrated 120mΩ High-Side Power MOSFET
- Integrated 85mΩ Low-Side Power MOSFET
- Low Noise Light Load Mode
- No External Compensation Required
- Very Low 90µA No-Load Operating Current
- <1µA Shutdown Current
- Up to 95% Efficiency
- 1.4MHz Switching Frequency
- Overload and Short-Circuit Protection
- Over-Temperature Protection
- Internal Voltage Ramped Soft-Start
- Temperature Range: -40°C to +85°C
- 16-pin 3mm x 4mm TDFN Package

Applications

- Digital Cameras and Camcorders
- Netbooks and Nettops
- Portable DVD and Media Devices
- Power-Over-Ethernet
- Set-Top Boxes

Typical Application

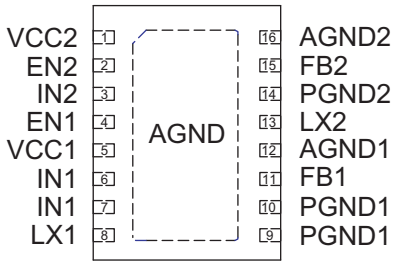


Pin Descriptions

Pin #	Name	Function
1	VCC2	Bias supply input for regulator #2.
2	EN2	Enable input for regulator #2. A logic high enables the second regulator of the AAT2522. A logic low forces regulator #2 into shutdown mode, placing the second output into a high-impedance state and reducing the VCC2 quiescent current to less than 1µA.
3	IN2	Power supply input for regulator #2.
4	EN1	Enable input for regulator #1. A logic high enables the primary regulator of the AAT2522. A logic low forces regulator #1 into shutdown mode, placing the primary output into a high-impedance state and reducing the VCC1 quiescent current to less than 1µA.
5	VCC1	Bias supply input for regulator #1.
6-7	IN1	Power supply input for regulator #1.
8	LX1	Inductor switching node for regulator #1. LX1 is the drain of the internal high-side P-channel and low-side N-channel MOSFETs. Externally connected to the power inductor as shown in the "Typical Application" drawing on page 1 of this datasheet.
9-10	PGND1	Power ground for regulator #1. PGND1 is internally connected to the source of the internal low-side N-channel MOSFET.
11	FB1	Feedback input for regulator #1. FB1 senses the output voltage for regulation control. Connect a resistive divider network from the output to FB1 to AGND1 to set the output voltage accordingly. The FB1 regulation threshold is 0.8V.
12	AGND1	Analog ground for regulator #1. AGND1 is internally connected to the analog ground of the control circuitry.
13	LX2	Inductor switching node for regulator #2. LX2 is the drain of the internal high-side P-channel and low-side N-channel MOSFETs. Externally connected to the power inductor as shown in the "Typical Application" drawing on page 1 of this datasheet.
14	PGND2	Power ground for regulator #2. PGND2 is internally connected to the source of the internal low-side N-channel MOSFET.
15	FB2	Feedback input for regulator #2. FB2 senses the output voltage for regulation control. Connect a resistive divider network from the output to FB2 to AGND2 to set the output voltage accordingly. The FB2 regulation threshold is 0.6V.
16	AGND2	Analog ground for regulator #2. AGND2 is internally connected to the analog ground of the control circuitry.
EP	AGND	Substrate analog ground.

Pin Configuration

TDFN34-16
(Top View)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
V_{IN1}, V_{IN2}	IN1 to PGND1, IN2 to PGND2	-0.3 to +6	V
V_{CC1}, V_{CC2}	VCC1 to AGND1, VCC2 to AGND2	-0.3 to +6	V
I_{INP1}, I_{INP2}	INPx RMS Current Capability	±3.0	A
V_{LX1}	LX1 to PGND1	-0.3 to (V_{IN1} + 0.3)	V
V_{LX2}	LX2 to PGND2	-0.3 to (V_{IN2} + 0.3)	V
I_{LX1}, I_{LX2}	LX RMS Current Capability	±5.0	A
V_{EN1}, V_{EN2}	EN1 to AGND1, EN2 to AGND2	-0.3 to V_{IN}	V
V_{FB1}	FB1 to AGND1	-0.3 to (V_{FB1} + 0.3)	V
V_{FB2}	FB2 to AGND2	-0.3 to (V_{FB2} + 0.3)	V
V_{GND}	AGND1 to PGND1, AGND2 to PGND2	-0.3 to +0.3	V

Thermal Characteristics

Symbol	Description	Value	Units
T_A	Ambient Temperature Range	-40 to +85	°C
T_J	Operating Junction Temperature Range	-40 to +150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec.)	300	°C
Power SO-10 Thermal Impedance			
θ_{JA}	Maximum Junction-to-Ambient Thermal Resistance	50	°C/W
P_D	Maximum Power Dissipation	2	W

Electrical Characteristics

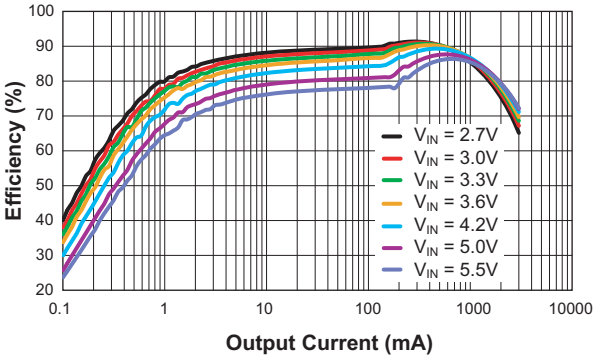
C_{IN} = 10µF, C_{OUT} = 22µF, L = 1.5µH. VIN1 = VIN2 = 3.6V, IN1 = VCC1 = EN1, IN2 = VCC2 = EN2, AGND = PGND. T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.7		5.5	V
V_{OUT}	Output Voltage Range		0.6		V_{IN}	V
	Output Voltage Tolerance	I_{OUT} = 0 to 3A, V_{IN} = 2.7V to 5.5V	-3.0		+3.0	%
V_{FB}	FB Regulation Threshold	No Load, T_A = 25°C	591	600	609	mV
I_Q	No Load Supply Current	Including IN1, VCC1, IN2, and VCC2 supply currents; No Load Current; not switching		90	180	µA
I_{SHDN}	Shutdown Current	EN = GND			1.0	µA
I_{FB}	FB Leakage Current	V_{FB} = 1.0V			200	nA
$\Delta V_{OUT(LOAD)}$	Load Regulation	0A to 3A Load		0.5		%
$\Delta V_{OUT}/V_{IN}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.2		%/V
f_{OSC}	Oscillator Frequency			1.40		MHz
t_{SS}	Soft-Start Period			150		µs
Protection Features						
V_{UVLO}	Input Under-Voltage Lockout	V_{IN} Rising, Hysteresis = 0.25V			2.7	V
T_{SHDN}	Over-Temperature Shutdown Threshold	Hysteresis = 15°C		140		°C
MOSFETs						
$R_{DS(ON)HI}$	High-Side P-Channel MOSFET On-Resistance			120		mΩ
I_{LIMPK}	High-Side P-Channel MOSFET Current Limit		3.6[1]			A
$R_{DS(ON)LO}$	Low-Side N-Channel On-Resistance			85		mΩ
Logic Input/Output Pins						
V_{EN}	EN Input Logic Threshold		0.6		1.4	V
I_{EN}	EN Input Current	0V, V_{IN}	-1.0		+1.0	µA

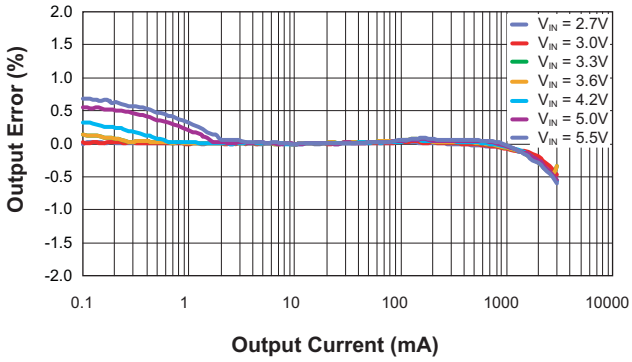
1. Specified by design.

Typical Characteristics

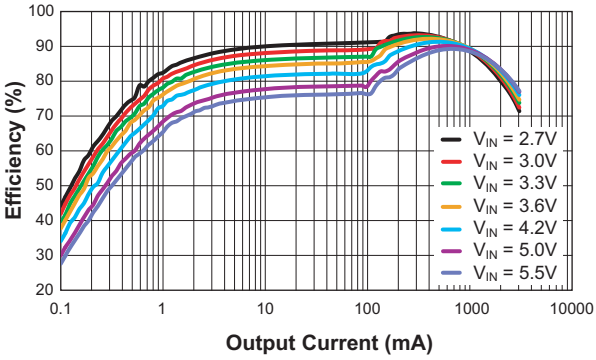
Step-Down Converter Efficiency vs. Load
(V_{OUT} = 1.2V; L = 1.2µH)



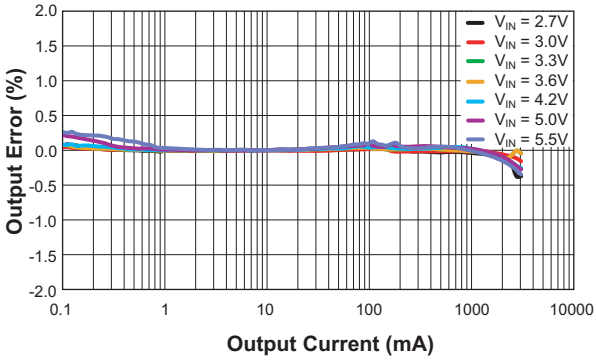
Step-Down Converter DC Regulation
(V_{OUT} = 1.2V; L = 1.2µH)



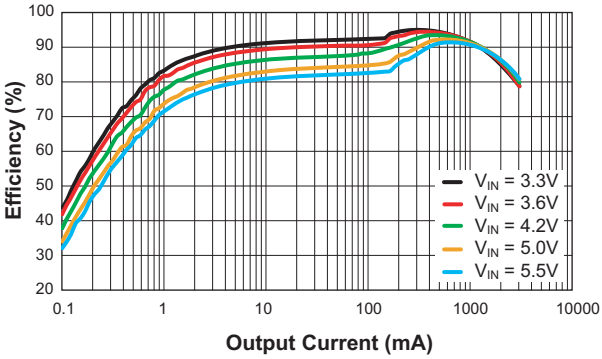
Step-Down Converter Efficiency vs. Load
(V_{OUT} = 1.8V; L = 1.8µH)



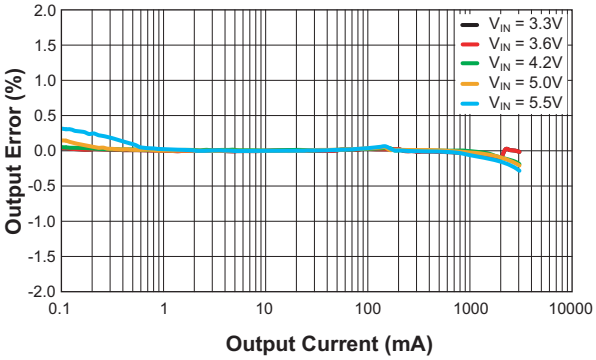
Step-Down Converter DC Regulation
(V_{OUT} = 1.8V; L = 1.8µH)



Step-Down Converter Efficiency vs. Load
(V_{OUT} = 2.5V; L = 2.5µH)

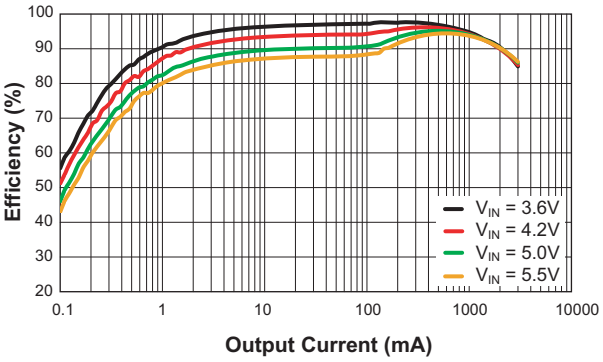


Step-Down Converter DC Regulation
(V_{OUT} = 2.5V; L = 2.5µH)

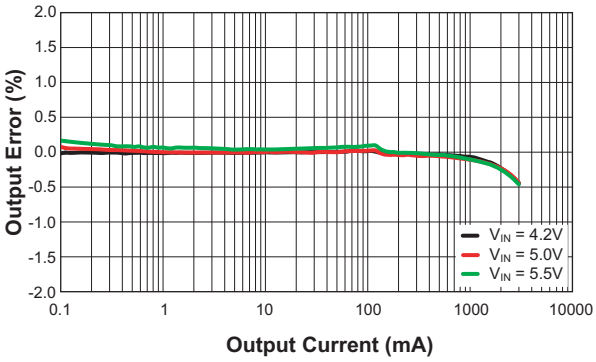


Typical Characteristics

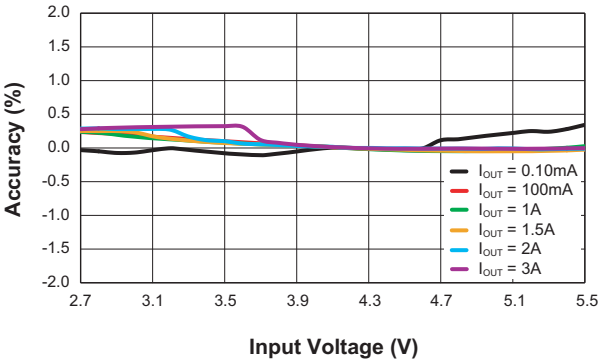
Step-Down Converter Efficiency vs. Load
(V_{OUT} = 3.3V; L = 3.3µH)



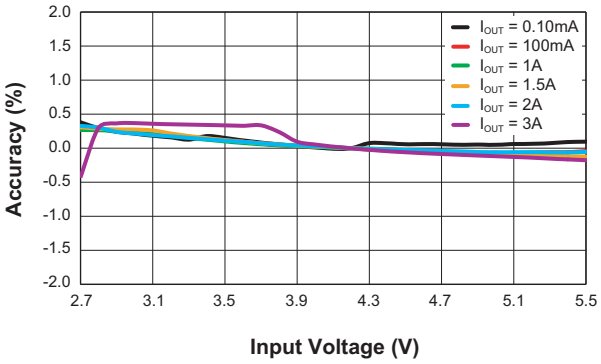
Step-Down Converter DC Regulation
(V_{OUT} = 3.3V; L = 3.3µH)



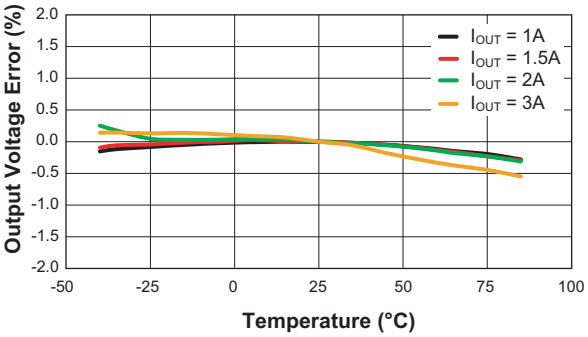
Step-Down Converter Line Regulation
(V_{OUT} = 1.2V; L = 1.2µH)



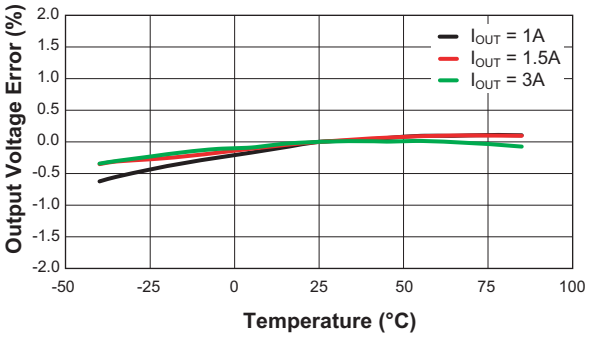
Step-Down Converter Line Regulation
(V_{OUT} = 1.8V; L = 1.8µH)



Step-Down Converter Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.2V)

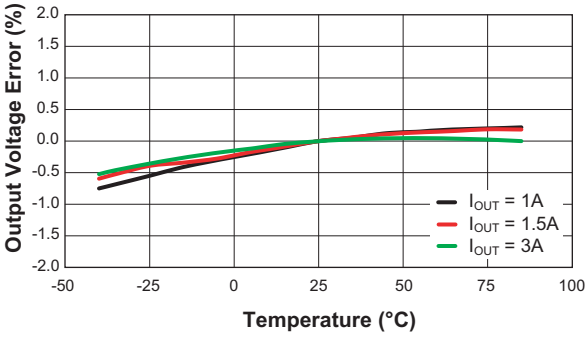


Step-Down Converter Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V)

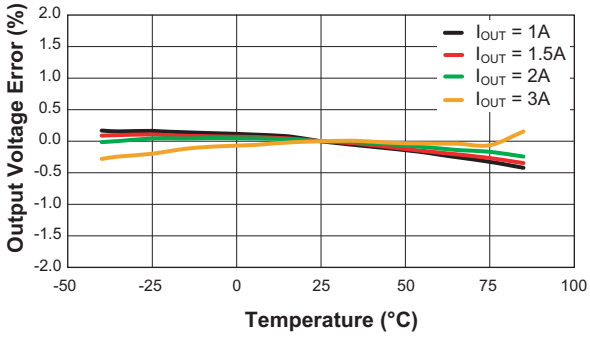


Typical Characteristics

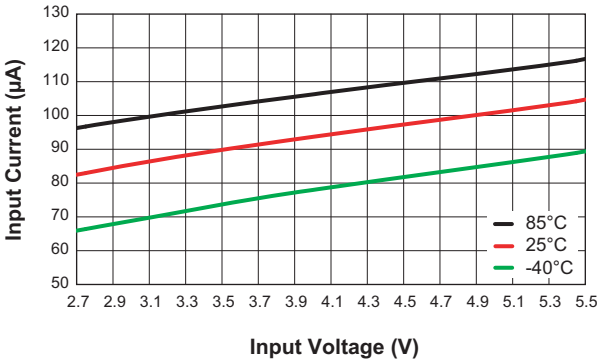
Step-Down Converter Output Voltage Error vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 2.5V)



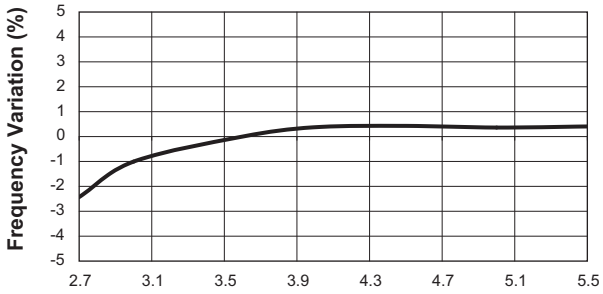
Step-Down Converter Output Voltage Error vs. Temperature
(V_{IN} = 4.2V; V_{OUT} = 3.3V)



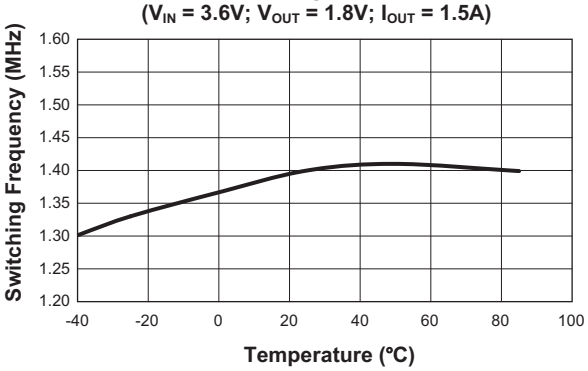
No Load Input Current vs. Input Voltage
(V_{EN1} = V_{EN2} = V_{IN})



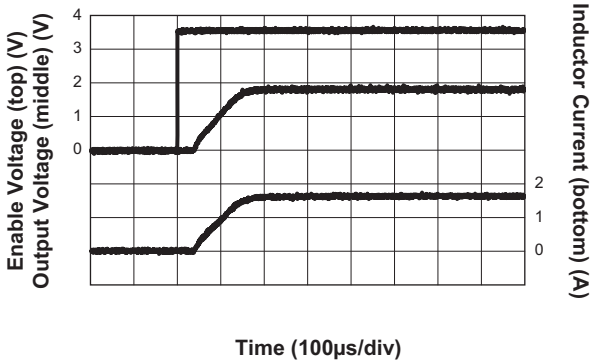
Step-Down Converter Switching Frequency vs. Input Voltage
(V_{OUT} = 1.8V; I_{OUT} = 1.5A)



Step-Down Converter Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1.5A)

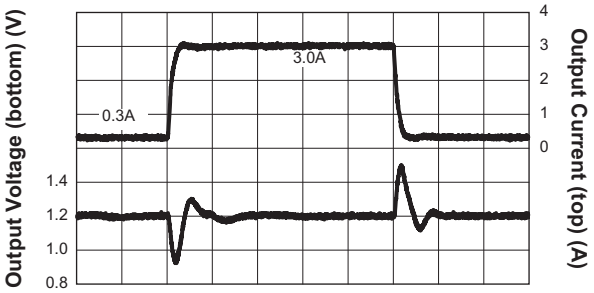


Step-Down Converter Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 1.5A; C_{FF} = 100pF)



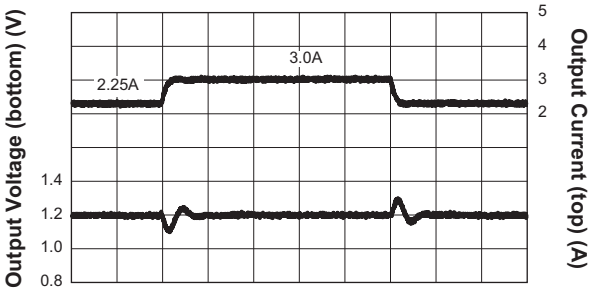
Typical Characteristics

Step-Down Converter Load Transient Response
(I_{OUT} = 0.3A to 3.0A; V_{IN} = 3.6V; V_{OUT} = 1.2V; C_{OUT} = 22µF)



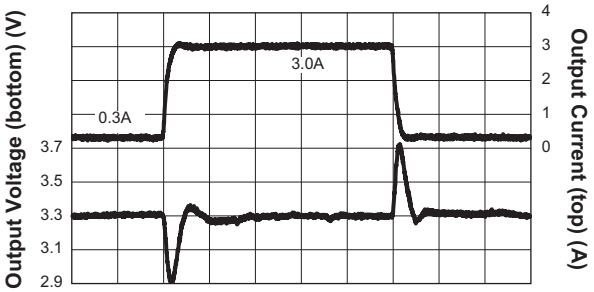
Time (100µs/div)

Step-Down Converter Load Transient Response
(I_{OUT} = 2.25A to 3.0A; V_{IN} = 3.6V; V_{OUT} = 1.2V; C_{OUT} = 22µF)



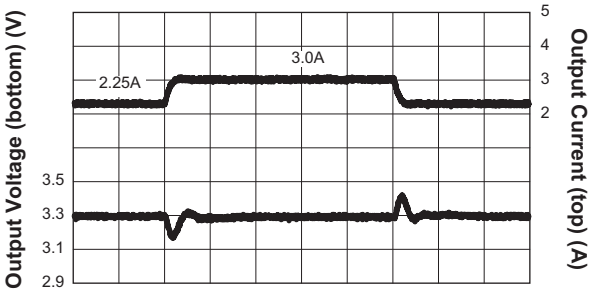
Time (100µs/div)

Step-Down Converter Load Transient Response
(I_{OUT} = 0.3A to 3.0A; V_{IN} = 4.2V; V_{OUT} = 3.3V; C_{OUT} = 22µF)



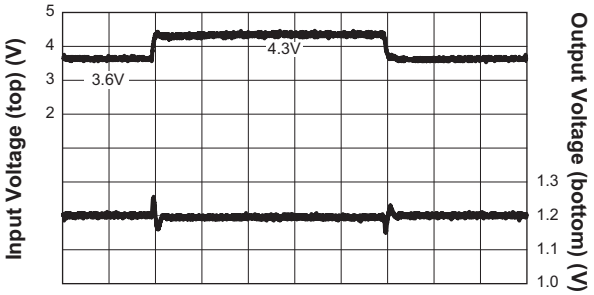
Time (100µs/div)

Step-Down Converter Load Transient Response
(I_{OUT} = 2.25A to 3.0A; V_{IN} = 4.2V; V_{OUT} = 3.3V; C_{OUT} = 22µF)



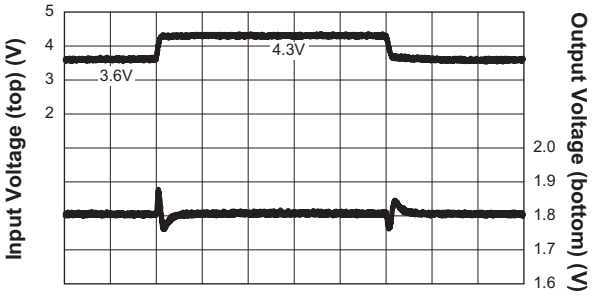
Time (100µs/div)

Step-Down Converter Line Transient Response
(V_{IN} = 3.6V to 4.3V; V_{OUT} = 1.2V; I_{OUT} = 3A)



Time (200µs/div)

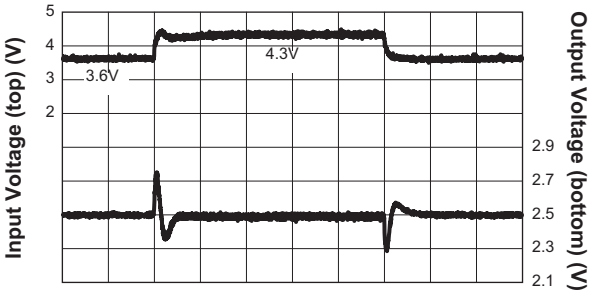
Step-Down Converter Line Transient Response
(V_{IN} = 3.6V to 4.3V; V_{OUT} = 1.8V; I_{OUT} = 3A)



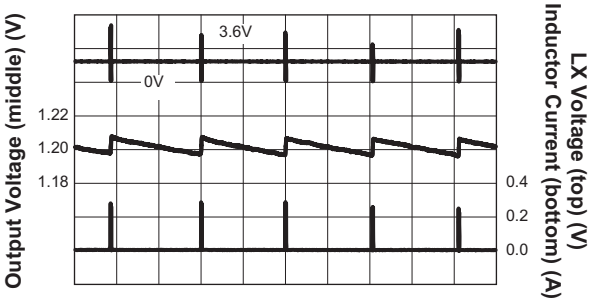
Time (100µs/div)

Typical Characteristics

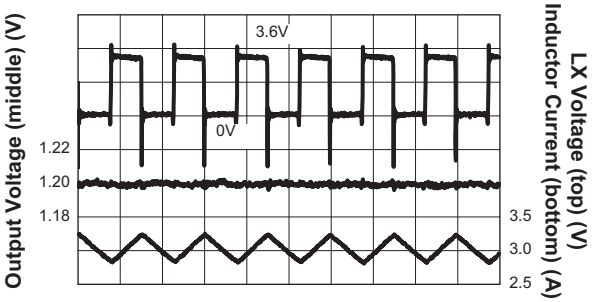
Step-Down Converter Line Transient Response
(V_{IN} = 3.6V to 4.3V; V_{OUT} = 2.5V; I_{OUT} = 3A)



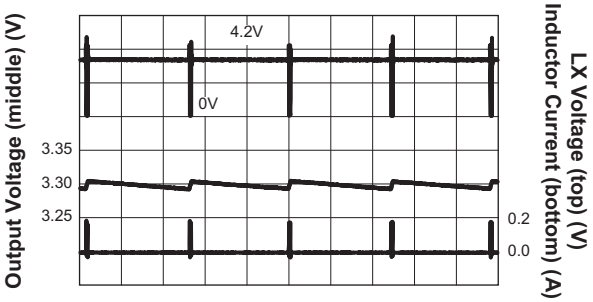
Step-Down Converter Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.2V; I_{OUT} = 1mA)



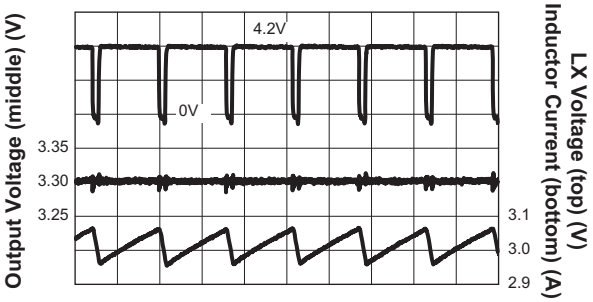
Step-Down Converter Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.2V; I_{OUT} = 3A)



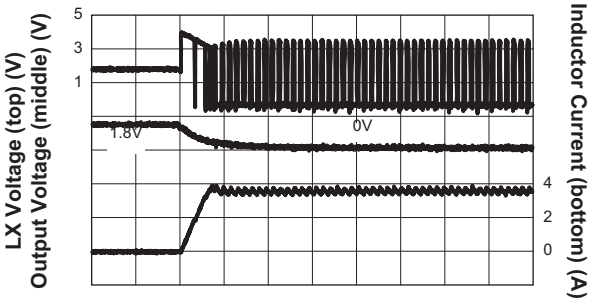
Step-Down Converter Output Ripple
(V_{IN} = 4.2V; V_{OUT} = 3.3V; I_{OUT} = 1mA)



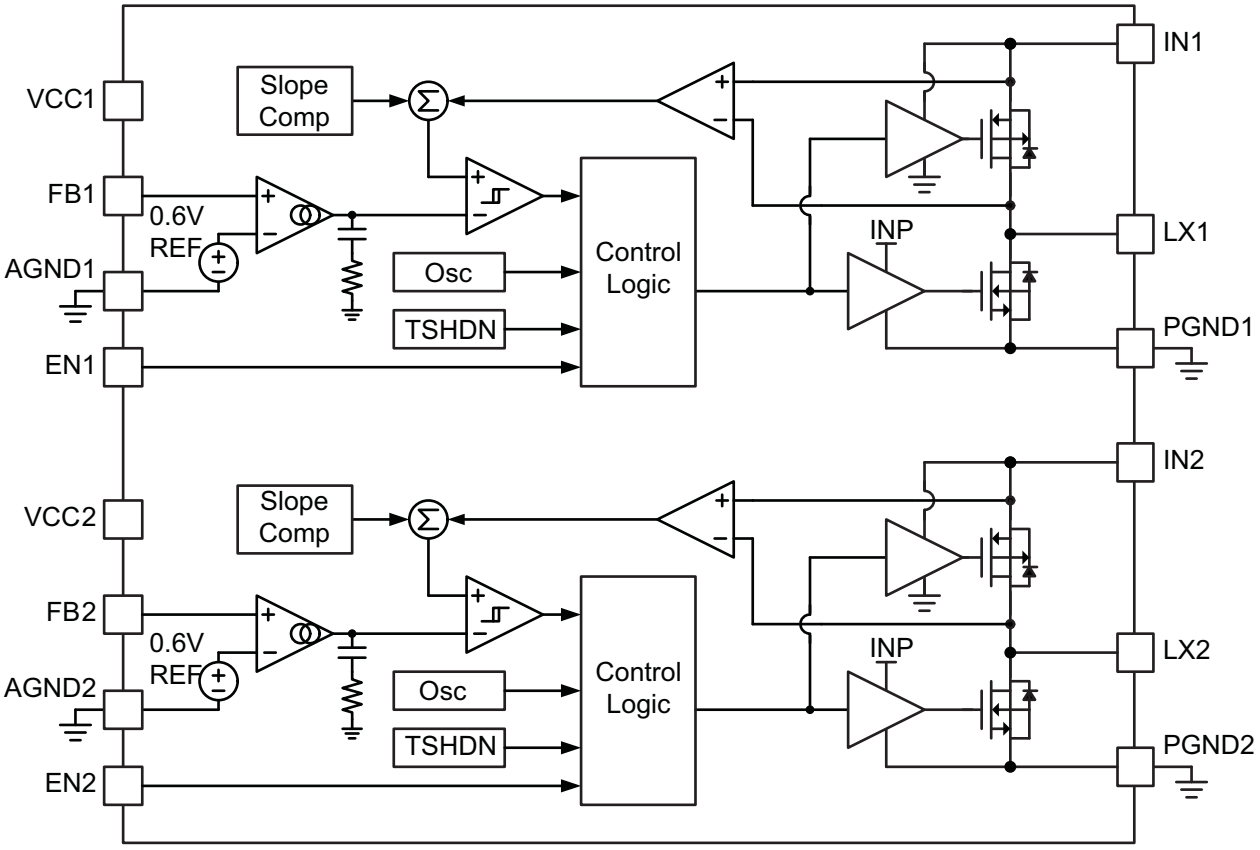
Step-Down Converter Output Ripple
(V_{IN} = 4.2V; V_{OUT} = 3.3V; I_{OUT} = 3A)



Step-Down Converter Short Circuit Protection
(V_{IN} = 5V; V_{OUT} = 1.8V; C_{FF} = 100pF)



Functional Block Diagram



Functional Description

The AAT2522 dual step-down regulators provide high-performance operation with a 1.4MHz switching frequency. The AAT2522 regulators are completely independent, including separate power supply inputs and enable signals. The highly integrated controller minimizes the external component requirements, optimizes efficiency over the complete load range, and produces reduced ripple and spectral noise. Apart from the small bypass input capacitor, only a small LC filter is required at the output. Typically, a 3.3µH inductor and a 22µF ceramic capacitor are recommended for a 3.3V output (see table of recommended values).

At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the high-side P-channel MOSFET (plus the DC drop of the external inductor and PCB layout). The device integrates extremely low $R_{DS(ON)}$ MOSFETs to achieve low dropout voltage during 100% duty cycle operation. This is advantageous in applications requiring high output voltages (typically > 2.5V) at low input voltages.

The integrated low-loss MOSFET switches can provide greater than 85% efficiency at full load (5V Input to 3.3V Output). Light-load, low-noise operation maintains high efficiency, low ripple and low spectral noise with low current conditions (typically < 150mA).

In battery-powered applications, as V_{IN} decreases, the converter dynamically adjusts the operating frequency prior to dropout to maintain the required high duty-cycle and maintain accurate output regulation. The regulators will maintain output regulation until either the dropout voltage limit is exceeded, or the input under-voltage threshold is reached.

The AAT2522 typically achieves better than ±0.5% output regulation across the input voltage and output load range. A current limit of 4.0A (typical) protects the IC and system components from short-circuit damage. Typical no load quiescent current is 90µA.

Thermal protection completely disables switching when the maximum junction temperature is detected. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Peak current mode control and optimized internal compensation provide high loop bandwidth and excellent response to input voltage and fast load transient events. Soft start eliminates output voltage overshoot when the enable or the input voltage is applied. Under-voltage lockout prevents spurious start-up events.

Control Scheme

The AAT2522 regulators are peak current-mode, step-down converters. The controller senses the current through the high-side P-channel MOSFET for current loop control, as well as short-circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The resulting peak current-mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current-mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The reference voltage is internally set to program the converter output voltage greater than or equal to 0.6V.

Soft-Start / Enable

Soft-start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT2522 into a low-power non-switching state. The total input current during shutdown is less than 1µA.

Protection Circuitry

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Input Under-Voltage Lockout

Internal bias of all circuits is controlled via the VCC input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Component Selection

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. Therefore, the inductor should be set equal to the output voltage numeric value in µH. This guarantees that there is sufficient internal slope compensation.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 3.3µH CDRH6D38NP series Sumida inductor has a 15mΩ worst case DCR and a 3.5A DC current rating. With a 3A load, the inductor DCR conduction loss is 135mW, which gives less than 1.4% loss in efficiency for a 3A, 3.3V output.

Output Capacitor Selection

The output capacitor limits the output ripple and provides holdup during large load transitions. A 10µF to 22µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop

responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The first-order relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_O}{V_{DROOP} \cdot f_{SW}}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 10µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

Input Capacitor Selection

Select a 10µF to 22µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PK-PK}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage (V_{IN} = 2x V_O):

$$C_{IN} = \frac{D \cdot (1 - D)}{\left(\frac{V_{PKPK}}{I_O} - ESR\right) \cdot f_{SW}} \text{ and } D = \frac{V_O}{V_{IN}}$$

The peak ripple voltage occurs when V_{IN} = 2x V_O (50% duty cycle), resulting in a minimum output capacitance recommendation:

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PKPK}}{I_O} - ESR\right) \cdot 4 \cdot f_{SW}}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the derated capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{D \cdot (1 - D)}$$

$$I_{RMS} = I_O \cdot \sqrt{\left(\frac{V_O}{V_{IN}}\right) \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current:

$$I_{RMS(MAX)} = \frac{I_O}{2} \text{ occurs when } V_{IN} = 2 \cdot V_O$$

The term D (1-D) appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2522. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in the Layout section of this datasheet (see Figure 3).

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or alu¬minum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Adjustable Feedback Network

The output voltage on the AAT2522 is programmed with external resistors R_{OUT-FB} and R_{FB-GND}. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, mak-

ing it more sensitive to external noise and interference. Therefore, the recommended value range for R_{FB-GND} (R3 and R5 in Figure 2) is 100kΩ for good noise immunity or 221kΩ for reduced no load input current.

The external resistor R_{OUT-FB} (R2 and R4 in Figure 2), combined with an external 100pF feed forward capacitor (C_5 and C_6 in Figure 2), delivers enhanced transient response for extreme pulsed load applications and reduces ripple in light load conditions. The addition of the feed forward capacitor typically requires a larger output capacitor (C_{OUT}) for stability. The external resistors set the output voltage according to the following equation:

$$V_O = 0.6V \cdot \left(1 + \frac{R_{OUT-FB}}{R_{FB-GND}}\right)$$

or solving for R_{OUT-FB}

$$R_{OUT-FB} = \left(\frac{V_O}{0.6V} - 1\right) \cdot R_{FB-GND}$$

V_{OUT} (V)	R3 = R5= 100kΩ R2 = R4 (kΩ)
1.0	65.5
1.2	100
1.5	150
1.8	200
2.2	267
2.5	316
3.3	453
4.2	604
4.6	655
5	806

Table 1: Step-Down Converter Feedback Resistor Selection for Different Output Voltages.

The typical circuit shown in the AAT2522 evaluation schematic is intended to be general purpose and suitable for most applications. In applications where transient load steps are more severe and the restriction on output voltage deviation is more stringent. To handle these cases some simple adjustments can be made. The schematic in Figure 2 shows the configuration for improved transient response in an application where the output is stepped down to 1.2V. The adjustments consist of adding an additional 22µF output capacitor, increasing the value of the feed forward capacitor C6 to 1nF, and adding the bias RC filter networks R1, C3 and R6, C4 in Figure 2.

Applications Information

Thermal Calculations

There are three types of losses associated with the AAT2522 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices:

$$P_{LOSS(RES)} = I_O^2 \cdot \left[R_{DS(ON)H} \cdot \left(\frac{V_O}{V_{IN}}\right) + R_{DS(ON)L} \cdot \left(\frac{V_{IN} - V_O}{V_{IN}}\right)\right]$$

Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the switching losses is given by:

$$P_{LOSS(SW)} = t_{SW} \cdot f_{SW} \cdot I_O \cdot V_{IN}$$

The term t_{SW} is used to estimate the full load step-down converter switching losses. Finally, the losses associated with the controller bias requirements are based the regulator's quiescent current (I_Q):

$$P_{LOSS(BIAS)} = I_Q \cdot V_{IN}$$

Summing the three power loss terms together provides the total power loss that the AAT2522 package must dissipate:

$$P_{TOTAL} = P_{LOSS(RES)} + P_{LOSS(SW)} + P_{LOSS(BIAS)}$$

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)H} = \left(\frac{V_O}{V_{IN}}\right) + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN34-16 package, which is 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \theta_{JA} + T_{AMB}$$

Assuming the operating ambient temperature is 85°C (the worst case), the maximum power dissipation for the TDFN34-16 package is determined in the following equation:

$$P_{MAX} = \frac{T_{J(MAX)} - T_{AMB}}{\theta_{JA}} \quad \frac{140°C - 85°C}{50°C/W} = 1.1W$$

The power dissipation varies with the duty cycle and the output current of the converters. Given the maximum power dissipation of the TDFN34-16 package at 25°C and 85°C, the relationship between the maximum allowable load for each channel and percent duty cycle are expressed in Figure 1.

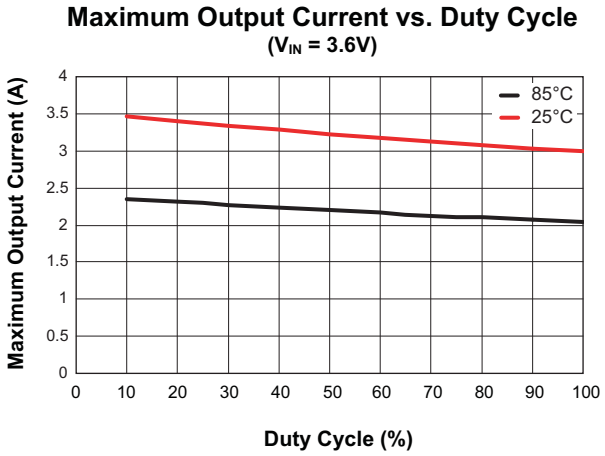


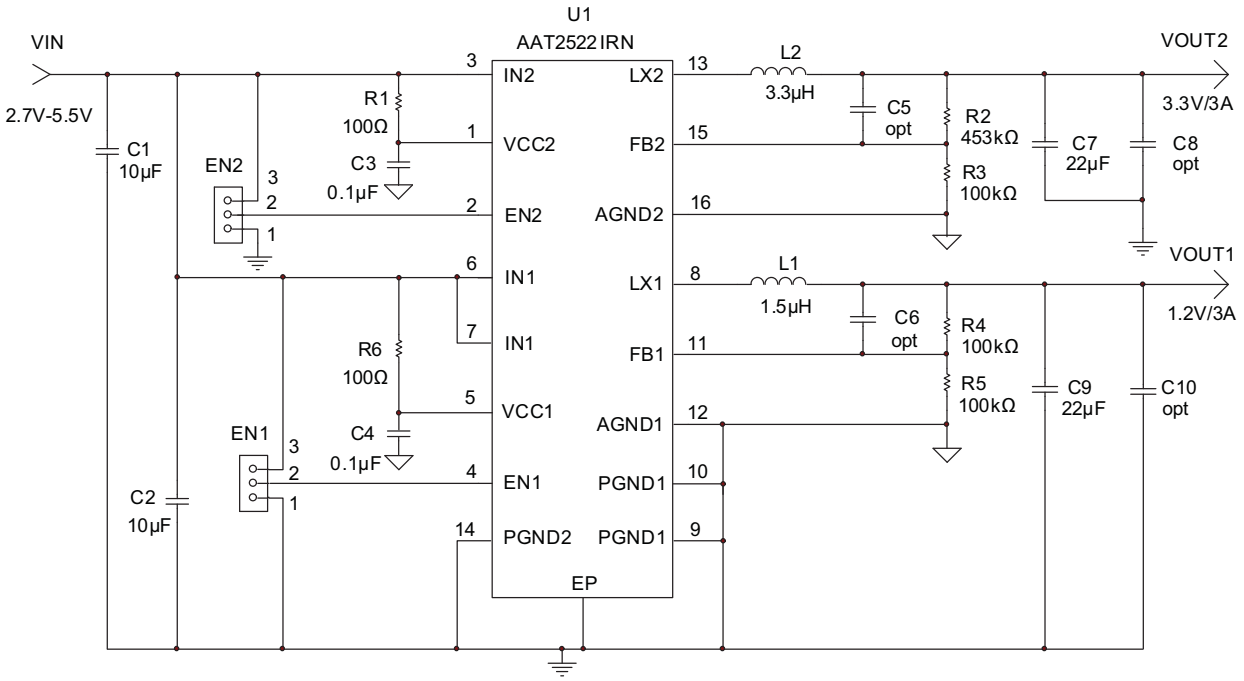
Figure 1: Maximum Allowable Current for AAT2522 Step-Down Converters.

As illustrated in Figure 1, the load limitation varies with the percentage of duty cycle and the operating ambient temperature. The total maximum load for both channels running at the same time in an 85°C ambient is about 4A (2A per channel). Therefore, if channel 1 is running at 1A, the maximum allowable load for channel 2 is no more than 3A to prevent the thermal shutdown. However, the maximum allowable load for each channel running at room temperature can increase up to 3A. In high current applications, the exposed pad needs to be connected to a thick power ground plane through vias for thermal dissipation.

Layout Recommendations

The suggested PCB layout for the AAT2522 is shown in Figures 3 and 4. The following guidelines should be used to help ensure a proper layout.

1. Place the input capacitor (C_{IN}) as closely as possible to VIN and PGND. Split the input supply tray to separate the two input capacitors in order to prevent noise coupling between two channels at heavy load.
2. The output capacitor and inductor should be connected as closely as possible. The inductor connection to the LX pin should be as short as possible.
3. The feedback trace or FB pin should be separated from any power trace and connected as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
4. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect unused signal pins to ground to avoid unwanted noise coupling.



U1	AAT2522IRN AnalogicTech, TDFN34-16
C1, C2	Ceramic cap, MLC, 10µF/10V, 0803
C3, C4	Ceramic cap, MLC, 0.1µF/10V, 0402
C5, C6	Ceramic cap, MLC, 100pF/10V, 0402, optional
C7-C9	Ceramic cap, MLC, 22µF/10V, 0805
L1	1.5µH, Sumida, CDRH4D22HPNP-1R5NC, 3.9A, 25mΩ
L2	3.3µH, Sumida, CDRH6D38NP-3R3N, 3.5A, 15mΩ
R1-R6	Carbon film resistor, 0402

Figure 2: AAT2522 Evaluation Board Schematic and Bill of Materials.

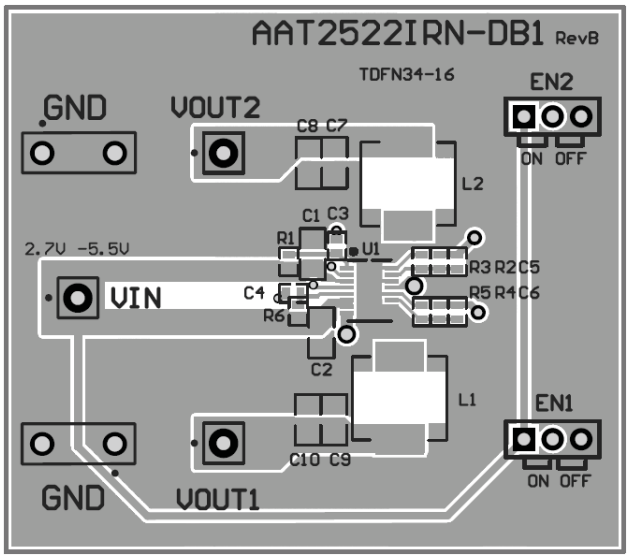


Figure 3: AAT2522 Evaluation Board Top Side Layout.

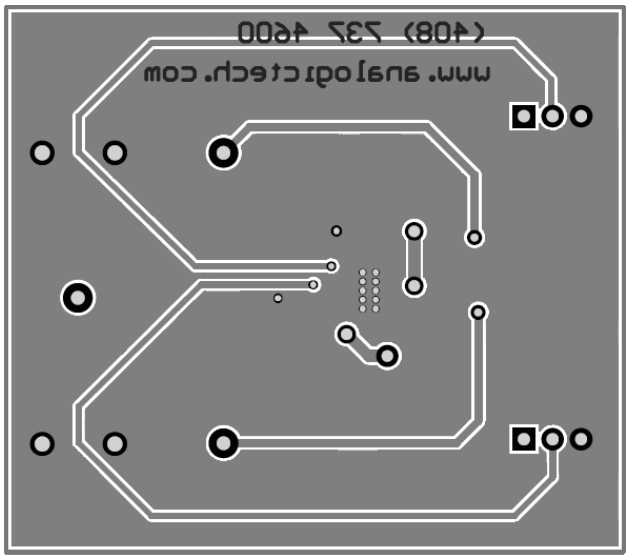


Figure 4: AAT2522 Evaluation Board Bottom Side Layout.

AAT2522 Design Example

Specifications

V_{OUT1} = 3.3V @ 1A, Pulsed Load ΔIL_{OAD} = 1A
V_{OUT2} = 1.2V @ 2A, Pulsed Load ΔI_{LOAD} = 2A
V_{IN1} = 3.6V
F_S = 1.4MHz
T_{AMB} = 85°C in TDFN34-16 Package

Step-Down Converter Output Inductor

The internal slope compensation for the AAT2522 is set to 75% of the inductor current down slope for a 1.8V output and 1.8µH inductor:

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{1.8\mu H} = 0.75 \frac{A}{\mu s}$$

For 3.3V and 1.2V outputs, the inductor values are given in the following equations:

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 3.3V}{0.75A \frac{A}{\mu s}} = 3.3\mu H; \text{ use } 3.3\mu H$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 1.2V}{0.75A \frac{A}{\mu s}} = 1.2\mu H; \text{ use } 1.5\mu H$$

For Sumida inductor, CDRH6D38NP-3R3N, 3.3µH, I_{SAT} = 3.5A, DCR = 15mΩ.

For Sumida inductor, CDRH4D22HPNP-1R5NC, I_{SAT} = 3.9A, 1.5µH, DCR = 25mΩ.

$$\Delta I_1 = \frac{V_{OUT1}}{L_1 \cdot F_S} \cdot \left(1 - \frac{V_{OUT1}}{V_{IN}}\right) = \frac{3.3V}{3.3\mu H \cdot 1.4MHz} \cdot \left(1 - \frac{3.3V}{3.6V}\right) = 0.06A$$

$$\Delta I_2 = \frac{V_{OUT2}}{L_1 \cdot F_S} \cdot \left(1 - \frac{V_{OUT2}}{V_{IN}}\right) = \frac{1.2V}{1.2\mu H \cdot 1.4MHz} \cdot \left(1 - \frac{1.2V}{3.6V}\right) = 0.476A$$

$$I_{PK1} = I_{OUT1} + \frac{\Delta I_1}{2} = 1A + 0.03A = 1.03A$$

$$I_{PK2} = I_{OUT2} + \frac{\Delta I_2}{2} = 2A + 0.476A = 2.5A$$

Step-Down Converter Output Capacitor

V_{DROOP} = 0.2V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 2A}{0.2V \cdot 1.4MHz} = 21.4\mu F; \text{ use } 22\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT2} \cdot (V_{IN(MAX)} - V_{OUT2})}{L \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.2V \cdot (5.5V - 1.2V)}{1.5\mu H \cdot 1.4MHz \cdot 5.5V} = 129mA_{RMS}$$

$$P_{RMS} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot (129mA)^2 = 83\mu W$$

Step-Down Converter Input Capacitor

Input Ripple V_{PP} = 50mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{50mV}{0.2A} - 5m\Omega\right) \cdot 4 \cdot 1.4MHz} = 9\mu F; \text{ use } 10\mu F$$

$$I_{RMS} = \frac{I_{OUT}}{2} = 1A$$

$$P = ESR \cdot (I_{RMS}^2) = 5m\Omega \cdot (1A)^2 = 5mW$$

AAT2522 Losses

All values assume at 85°C ambient temperature and thermal resistance of 50°C/W in the TDFN34-16 package.

$$P_{TOTAL} = \frac{I_{OUT1}^2 \cdot (R_{DS(ON)H} \cdot V_{OUT1} + R_{DS(ON)L} \cdot [V_{IN} - V_{OUT1}])}{V_{IN}} + (t_{sw} \cdot F_S \cdot I_{OUT1} + I_{Q1}) \cdot V_{IN}$$
$$+ \frac{I_{OUT2}^2 \cdot (R_{DS(ON)H} \cdot V_{OUT2} + R_{DS(ON)L} \cdot [V_{IN} - V_{OUT2}])}{V_{IN}} + (t_{sw} \cdot F_S \cdot I_{OUT2} + I_{Q2}) \cdot V_{IN}$$

$$P_{TOTAL} = \frac{1A^2 \cdot (0.12\Omega \cdot 3.3V + 0.085\Omega \cdot [3.6V - 3.3V])}{3.6V} + (5ns \cdot 1.4MHz \cdot 1A + 84\mu A) \cdot 3.6V$$
$$+ \frac{2A^2 \cdot (0.12\Omega \cdot 1.2V + 0.085\Omega \cdot [3.6V - 1.2V])}{3.6V} + (5ns \cdot 1.4MHz \cdot 2A + 84\mu A) \cdot 3.6V$$

$$P_{TOTAL} = 0.58W$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (50°C/W) \cdot 0.58mW = 114°C$$

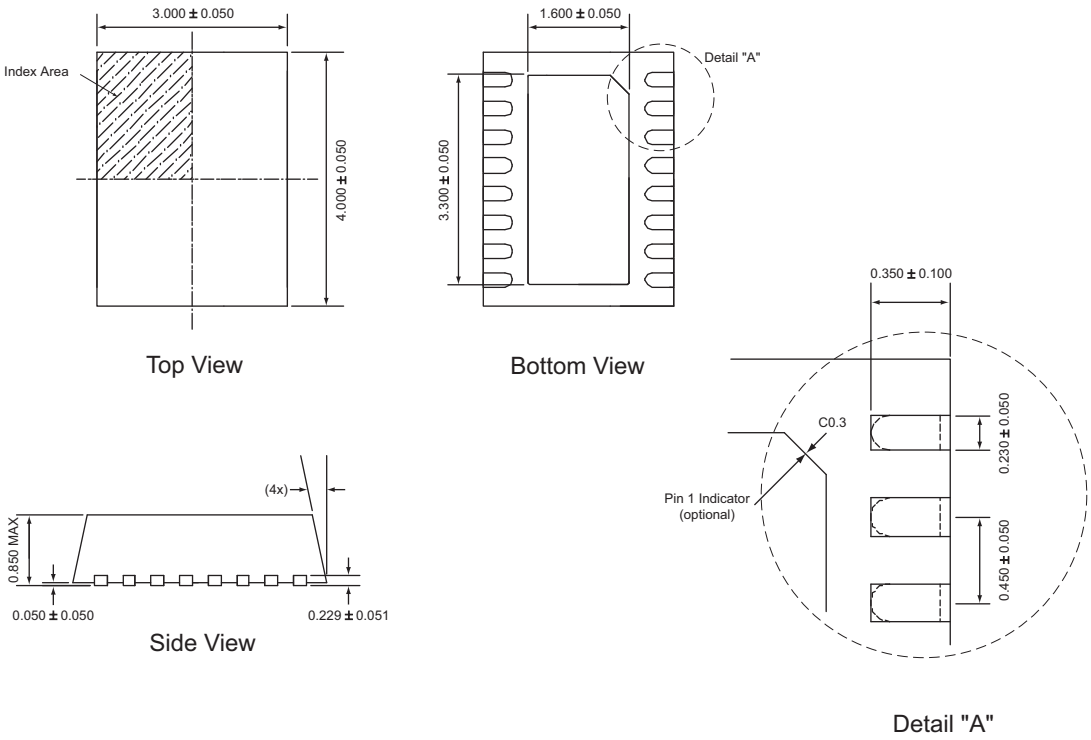
Ordering Information

Package	Marking	Part Number (Tape and Reel)[1]
TDFN34-16	9BXYY	**AAT2522IRN-1-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Package Information

TDFN34-16[2]



All dimensions in millimeters.

1. Sample stock is generally held on part numbers listed in **BOLD**.
2. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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